REMARKS

Claims 1-5, 7-16, 18-21 are pending in the present application. Claims 6 and 17 are cancelled herein. Claims 1, 7, 8, 10, 12, and 18 have been amended. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Claims 1-4, 6, 8-15, 17 and 20-21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurjanowicz et al. (U.S. Patent No. 6,894,941 B2, hereinafter "Kurjanowicz"), in view of a Feurle et al. (U.S. Patent Application No. 2003/0043674 A1, hereinafter "Feurle"). This rejection is hereby respectfully traversed.

With respect to independent claims 1 and 12, the Examiner remarked that Kurjanowicz teaches a method of reducing a rate for refreshing a portion of a dynamic access memory, comprising providing a first portion of said DRAM comprising a plurality of volatile memory cells (here the Examiner cited Col. 7, lines 26-38 and Col. 8, lines 33-36 and memory banks 102 and 108) permitting refresh at a first rate (here the Examiner cited the single cell per bit mode, Col. 15, lines 37-39) , and a second portion of said DRAM (here the Examiner cited upper memory bank 102 when the DRAM of Kurjanowicz operates in a short page access mode, and cited Col. 7 lines 26-45 and Col. 8 lines 33-36) comprising a plurality of volatile memory cells, permitting refresh at a second rate (Examiner states the Kurjanowicz second rate is taught in the disclosure of the "two bits per cell" mode that is lower than the first rate, and cites Col. 15 lines 40-43).

Claim 1, as amended herein, specifically recites:

> A method of reducing a rate for refreshing a portion of a dynamic random access memory (DRAM), comprising:
>
> providing a first portion of said DRAM comprising a plurality of volatile memory cells permitting refresh at a first rate and a second portion of said DRAM comprising a differing plurality of volatile memory cells permitting refresh at a second rate lower than said first rate;
>
> determining, by performing testing, the first and second refresh rates that are permitted for the first and second portions;
>
> storing information for distinguishing between said first portion and said second portion and storing information indicating the first and second refresh rates associated with the first and second portions within said DRAM; and
>
> accessing said stored information to determine when and to refresh said first portion at said first rate and to determine when and to refresh said second portion at said second rate.

Claim 12 is an apparatus claim that recites similar elements, although in apparatus form.

Applicant respectfully submits that Kurjanowicz does not, in fact, show, teach or suggest the elements of Claim 1 and similarly apparatus Claim 12. Kurjanowicz teaches a DRAM with input signals indicating two independent choices for modes of operation (see e.g. Col. 6, lines 39-44). First the SHORT PG input signal indicates whether the DRAM is to operate in short or long page mode (Col. 7, lines 26-33). In the short page mode, the DRAM is operated as two

access accesses both portions (See Figure 3, described at Col. 7, lines 33-45). Another input signal DIFF_MODE determines whether a single bit per cell mode or a dual bit per cell mode is used to store data. (Col. 8, lines 13-26). Kurjanowicz further teaches that these two modes are independent (Col. 13, lines 13-16; and see also Col. 8, lines 28-31) and, that in the dual bit per cell mode, a longer refresh time may be used. (Col. 13, lines 35-52).

Applicant submits, however, that there is no teaching anywhere in Kurjanowicz to store different refresh rates for the two portions within the DRAM as required by the claims. This is apparent because the entire DRAM in Kurjanowicz is refreshed at a single rate at all times. That is, either the entire DRAM is operated in a "two bit per cell" mode, in which mode the refresh may be performed at a lower rate, or the entire DRAM of Kurjanowicz is operated in a single bit per cell mode, in which instance the entire DRAM is refreshed at a higher rate. The short page and long page mode determine how many wordlines are active for a cycle, but the entire DRAM is in single bit per cell or dual bit per cell mode, irrespective of the page length. The primary reference does not teach the elements of Claims 1 and 12, and specifically does not teach the elements of providing two portions and storing information within the DRAM for distinguishing the first and second portions, determining first and second refresh rates for the two portions, and storing information within the DRAM indicating the first and second refresh rates.

The Examiner admits that Kurjanowicz is missing some of the elements of Claims 1 and 12; however, the Examiner still asserts that the Kurjanowicz reference does teach storing the information as recited in the claims. Applicant cannot agree with the findings of the Examiner.

The Examiner then adds the Feurle reference, which is co-owned by the owner of the present application. Feurle is added for disclosing the portions having different rates. However, Feurle discloses interrupting refresh cycles that are not needed for certain portions, and therefore

Feurle discloses interrupting refresh cycles that are not needed for certain portions, and therefore does not provide the missing elements of storing information indicating the refresh rates associated with a first and second portion. The controller of Feurle does not access stored information indicating refresh rates; instead a refresh cycle for a subportion is interrupted by logic. Therefore, even if the proposed combination is made, Feurle does not provide the elements missing from Kurjanowicz. Applicant concludes that the claims are nonobvious and allowable over the prior art references and the combination relied upon.

Claims 2-4 and 8-11 depend from and incorporate the elements of Claim 1, and are therefore also believed to be allowable. Dependent claim 6 is cancelled herein. Claims 13-15 and 20-21 depend from and incorporate the elements of Claim 12 and are therefore also believed to be allowable. Dependent claim 17 is cancelled herein. Reconsideration and allowance are therefore respectfully requested.

Claims 5 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurjanowicz and Feurle, in view of Klein, (U.S. Patent No. 6,838,331 B2, hereinafter "Klein"). This rejection is also hereby respectfully traversed.

Claim 5 depends from and incorporates the elements of Claim 1, and adds the elements of a sleep mode and an active mode to the portions of the DRAM. The Examiner adds Klein, which discloses a sleep mode, to the combination of Kurjanowicz and Feurle.

Applicants believe that the combination of Klein to the references previously discussed does not obviate the elements of Claim 1, the parent claim, and that therefore the dependent claim which incorporates allowable limitations of the parent claim is also allowable over the prior art relied upon. Reconsideration and allowance are therefore requested.

parent claim is believed to be allowable over the combination of the first two references, the addition of Klein does not cure the deficiencies of those references, and the dependent claim incorporates the allowable elements of Claim 12 and is therefore also allowable. Accordingly, reconsideration and allowance are respectfully requested for Claim 16.

Claims 7 and 18-19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurjanowicz, and Feurle, in view of Caulkins, (U.S. Patent No. 6,473,355 B2, hereinafter "Caulkins"). This rejection is also hereby respectfully traversed.

Claim 7 depends from Claim 1 and adds the limitation of non volatile storage for the information stored within the DRAM of Claim 1. Caulkins is recited for disclosing the non volatile storage. Applicant notes that Caulkins' non volatile storage is not provided within a DRAM as required by the claim, and so without agreeing that the required suggestion to combine these references exists, Applicant responds that even if the proposed combination was made as the Examiner suggests, Caulkins does not cure the deficiencies in the first two references and so the parent claim remains allowable over the prior art. Claim 7 necessarily incorporates these allowable limitations and so is also allowable over the rejection. Similarly, Claims 18-19 recite additional elements on the apparatus of Claim 12, particularly reciting storing information in non volatile memory, and so for the same reasons as for Claim 7, these dependent claims are believed to be allowable. Reconsideration and allowance for these claims over the rejection is therefore requested.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mark E. Courtney, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge, or credit any overpayment, Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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